Performance of RFMOS™ for 1.9 GHz CDMA Operation

Fred Brauchler, Marcel Tutt†, Dave Seymour, Ali Khatibzadeh, John Erdljac and John Arch
Texas Instruments, Dallas, Texas
† TriQuint Semiconductor, Dallas, Texas

Abstract

We report the first measured ACPR properties of Texas Instruments' RFMOS™ power transistor technology at 1.9 GHz. It demonstrated a 49% PAE with ACPR = -45 dBc for V_{DS} = 3.6V. The performance results are presented as a function of bias and tuning and demonstrate that the RFMOS™ technology has excellent potential for CDMA applications.

Introduction

Mobile digital wireless communications is undergoing dramatic growth at 1.9 GHz. Silicon CMOS technology is expected to have a cost advantage over Gallium Arsenide due to its high volume throughput capability. It also offers higher level of integration such as mixed signal, power management, and RF on a single chip. Texas Instruments' RFMOS™, a derivative of CMOS technology, has been successfully applied to GSM power amplifiers [1], which operate in a saturated mode. However, digital systems, such as CDMA, place great demands on the power amplifier (PA) performance because of the linearity specifications. To achieve the linearity requirements, the PA must operate backed-off from saturation where the greatest efficiency is obtained. This, in turn, results in reduced talk time. We present the first adjacent channel power ratio (ACPR) results for RFMOS™ which demonstrates its suitability for CDMA PA applications at 1.9 GHz and 3.6V.

Methodology

The process technology of the CMOS studied here is described elsewhere [1,2]. It features a 0.5 µm gate length and it has an f_T of 14 GHz and an F_{max} of 13 GHz. These excellent small signal properties indicate its suitability for use at 1.9 GHz. At this frequency, a transistor is capable of 12 dB gain at 65% PAE and 80 mW/mm output power [2]. Application to CDMA systems, however, also requires detailed knowledge of its power and ACPR characteristics. These characteristics were measured using an on-wafer load-pull system which features fully calibrated precision electromechanical tuners with an integrated digitally modulated source and a spectrum analyzer. Precise vector characterization of all components established the reference planes at the device pads. The 1.9 GHz test signal was modulated using an O-QPSK signal conforming to IS-95 specifications. Power ratio measurements of a 30 kHz bandwidth adjacent-channel at a 1.25 MHz offset to the 1.23 MHz bandwidth channel were used to determine ACPR (figure 1). Input/output power and gain were determined with a power meter. A single nominal transistor of gate width 1 mm was measured to generate all the data presented here. Separate tuning conditions of $\Gamma_S = 0.69<39$, $\Gamma_L = 0.35<128$ and $\Gamma_S = 0.67<47$, $\Gamma_L = 0.50<77$ were established for maximum power and maximum power added efficiency (PAE), respectively. The device is biased at a class A/AB operation with V_{DS} = 3.6V and I_{DS} = 20 mA. The ACPR was then measured at

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the same tuning conditions as a function of input power, drain voltage (1.6V to 4.3V) and a drain current (2 mA to 40 mA quiescent).

Experimental Results

Figures 2 and 3 display the PAE and ACPR vs. P_{out} for the 1 mm gate width device under the maximum efficiency and maximum output power tuning conditions, respectively, at the class A/AB bias of $V_{DS} = 3.6V$ and $I_{DS} = 20$ mA. Use of maximum PAE tuning increased the peak efficiency from approximately 53% to almost 60% compared to the maximum power tuning case. However, for a given ACPR, the efficiency is about the same. For example, for an ACPR = -45 dBc, the PAE increased to 34% from 33%.

Performance near class B operation was investigated. Figure 4 shows the PAE and ACPR vs P_{out} for the same tuning as figure 2, but with a lower bias, $V_{DS} = 3.6V$ and $I_{DS} = 2$ mA. As can be seen for the ACPR = -45 dBc condition, an efficiency of 49% was achieved at 30 mW output power. Such an improvement was not seen at the maximum power tuning condition. This demonstrates the advantages of using peak efficiency tuning for this CMOS technology.

The output power, PAE, and gain were further studied as a function of bias at the maximum efficiency tuning condition. Under a constant ACPR of -45 dBc, the PAE varied from 49% to 23% and the output power changed less than 1dB for I_{DS} varied from 2 mA to 40 mA (figure 5). These results show that a good ACPR can be obtained along with good efficiency by operating in a class AB mode with only a slight change in the output power. This demonstrates that RFMOS™ has very good potential for CDMA applications. Furthermore for the same ACPR = -45 dBc, a constant quiescent drain current of 20 mA, and V_{DS} varied from 2.8V to 4.4V, the gain remained essentially constant, however the PAE changed from 28% to 36% and the output power increased approximately 4 dB (figure 6). These results demonstrate the trade-off with drain current or drain voltage for -45 dBc ACPR in this CMOS technology.

Figure 7 displays PAE and output power vs. drain voltage for the same tuning and ACPR = -45 dBc. This plot shows how under the proper biasing conditions, >30% PAE can be obtained over a 15 dB output power range and satisfy the linearity requirement. This indicates that this technology can provide high efficiency even at a backed-off output power from the maximum output level, a desirable characteristic in a CDMA application [3]. This demonstrates Texas Instruments' RFMOS™ has excellent potential for CDMA applications at 1.9 GHz.

Conclusions

We presented the first power and ACPR studies of Texas Instruments' RFMOS™ for CDMA applications at 1.9 GHz. The results demonstrate that RFMOS™ provides good ACPR performance over a wide range of bias conditions. Tuning for maximum efficiency provided greater than 40% PAE with an ACPR of -45 dBc for class A/AB operation. Under the same tuning and ACPR conditions, reducing the drain current increases PAE to 49% with output power at 30 mW. Finally under the proper bias conditions, >30% PAE can be obtained for an output power range of 15 dB which is a desirable characteristic in CDMA applications.

References

[1] R. Culbertson, *et al*., "Evolution of RFMOS™ Power Amplifiers for High Efficiency Digital Cellular Applications," *Wireless Technology '98 Conference Digest*, (Feb 1998).

[2] A. Khatibzadeh, *et al*., "RF Technology Trends in Digital Wireless Communications," *Wireless Technology '98 Conference Digest*, (Feb 1998).

[3] J. Sevic, "Statistical Characterisation of RF Power Amplifier Efficiency for Wireless Communication Systems," 1997 Wireless Communications Conference, p.110-113.

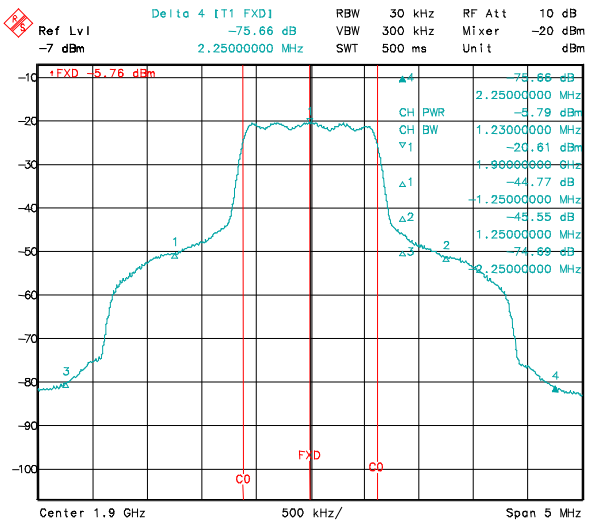

Figure 1. Measured output spectrum of a 0.5 µm gate length RFMOS™ transistor operating at an ACPR near -45 dBc.

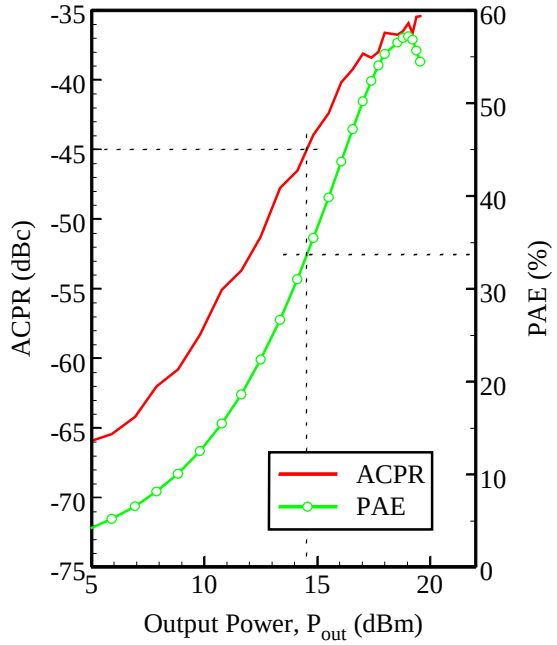

Figure 2. Measured PAE and ACPR vs. Output Power for a 0.5 µm gate length CMOS transistor with maximum efficiency tuning for V_{DS} = 3.6V and I_{DS} = 20 mA.

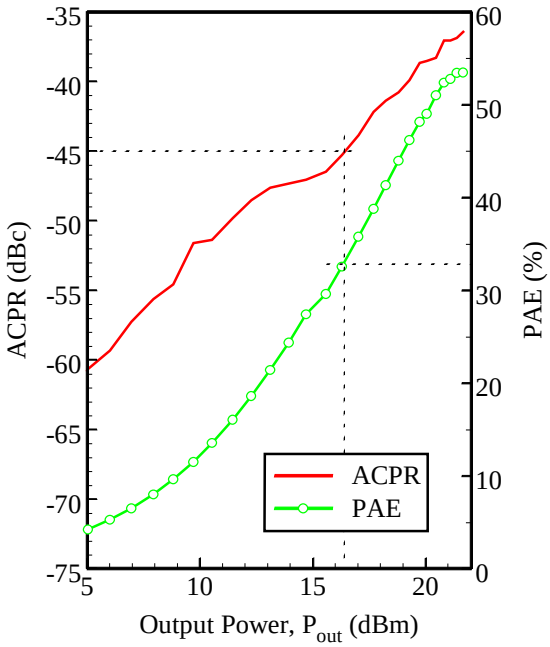

Figure 3. Measured PAE and ACPR vs. Output Power for a 0.5 µm gate length CMOS transistor with maximum power tuning for V_{DS} = 3.6V and I_{DS} = 20 mA.

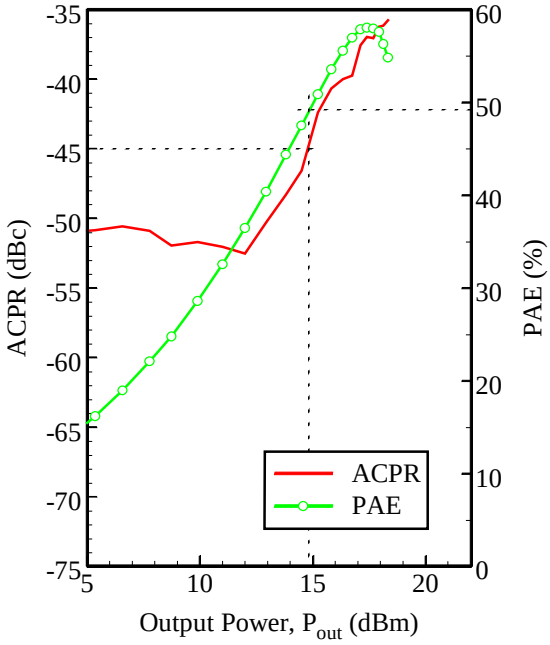

Figure 4. Measured PAE and ACPR vs. Output Power for a 0.5 µm gate length CMOS transistor with maximum efficiency tuning, but at V_{DS} = 3.6V and I_{DS} = 2 mA.

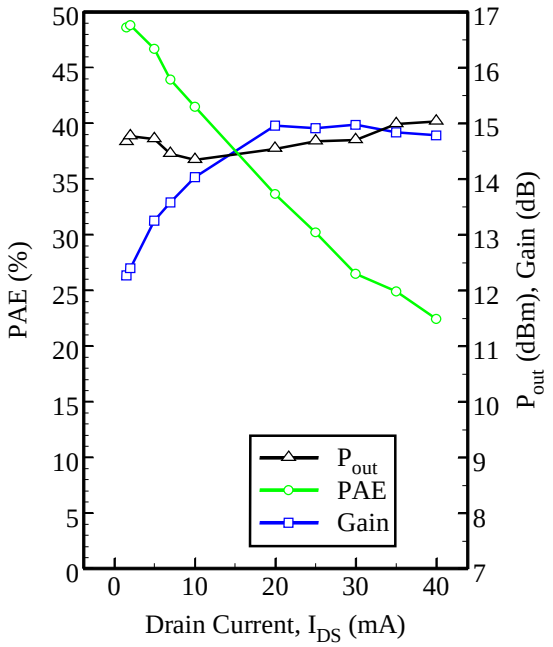

Figure 5. Measured efficiency, gain and output power vs. quiescent drain current for a 0.5 µm gate length CMOS transistor under a constant -45 dBc ACPR and 3.6V drain bias condition.

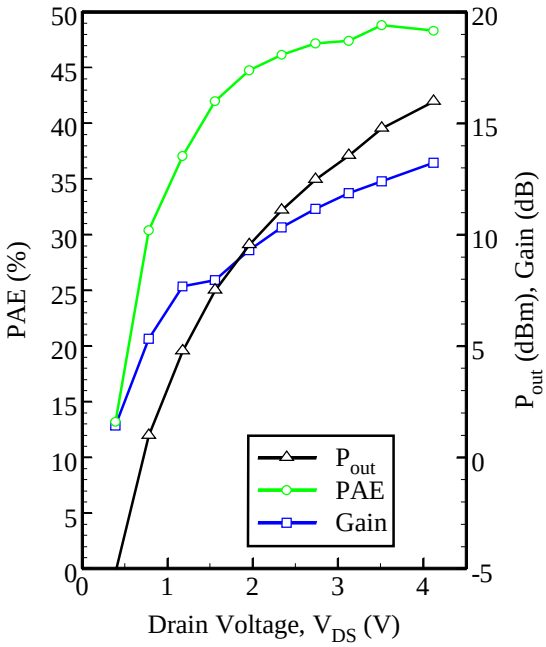

Figure 7. Measured efficiency and output power vs. drain voltage for a 0.5 µm gate length CMOS transistor under a constant -45 dBc ACPR. Bias conditions vary.

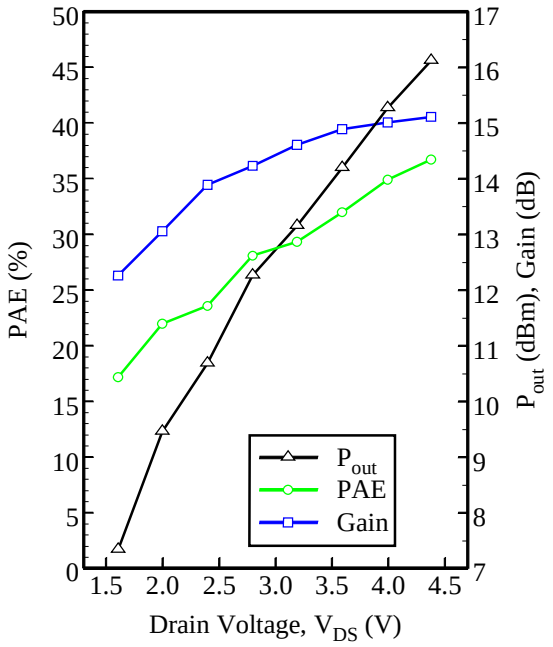

Figure 6. Measured efficiency, gain and output power vs. drain voltage for a 0.5 µm gate length CMOS transistor under a constant -45 dBc ACPR. Quiescent drain current is 20mA.